AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED REVISION TO 37 CFR 1.121)

Please cancel claim 5 without prejudice.

1. (CURRENTLY AMENDED) A method for generating superset pinouts for a family of devices, comprising the steps of:

(A) defining a pinlist for each device within said family of devices;

(B) generating a superset listing of pins from said pinlist;

(C) creating said superset pinout for said family of devices by eliminating potential footprint variations within said family of devices with said superset pinout; and

(D) marking each pin of said superset pinout associated with each member of said family of devices.

2. (ORIGINAL) The method according to claim 1, wherein step (D) further comprises;

customizing said superset pinout.

3. (ORIGINAL) The method according to claim 2, wherein step (D) further comprises:

marking a specific pinout for each member of said family of devices in response to the customizing.

4. (ORIGINAL) The method according to claim 1, wherein said family of devices comprises devices with combined programmable logic and high-speed serial channels.

5. (CANCEL)

6. (CURRENTLY AMENDED) The method according to claim 1, wherein step (C) further comprises:

eliminating potential layout variations within said family of devices with said superset pinout.

7. (CURRENTLY AMENDED) The method according to claim 1, wherein step (B) further comprises:

combining pins shared by more than one member of said family of devices.

8. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allocating a pin for each signal in said pinlist.

9. (CURRENTLY AMENDED) The method according to claim 1, wherein step (C) further comprises:

providing a footprint common to ~~members~~ each member of said family of devices.

10. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

accommodating needs common to members of said family of devices with said superset pinout.

11. (CURRENTLY AMENDED) The method according to claim 1, wherein step (C) further comprises:

limiting each ~~pin~~ of said superset listing of pins to a single function.

12. (CURRENTLY AMENDED) The method according to claim 1, wherein step (D) further comprises:

initiating said pins after said pinout is completed.

13. (ORIGINAL) The method according to claim 1, wherein step (D) further comprises:

marking one or more pins no-connect for a particular member device.

14. (ORIGINAL) The method according to claim 1, wherein said family of devices comprise programmable logic and high-speed serial channel devices.

15. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allowing for migration of devices within said family of devices.

16. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allowing for migration to higher gate densities.

17. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allowing for migration to increased bandwidth channels.

18. (CURRENTLY AMENDED) The method according to claim 1, wherein step (C) further comprises:

reducing layout and footprint changes on a board connected between said members of said family of devices.

19. (CURRENTLY AMENDED) An apparatus comprising:

means for generating superset pinouts for a family of devices;

means for defining a pinlist for each device within said family of devices;

means for generating a superset listing of pins from said pinlist by eliminating layout variations within said family of devices with said superset pinout;

means for creating said superset pinout for said family of devices; and

means for marking each pin of said superset pinout associated with each member of said family of devices.

20. (CURRENTLY AMENDED) An apparatus comprising:

a device configured to generate superset pinouts for a family of devices, wherein said device is further configured to define a pinlist for each device within said family of devices, generate a superset listing of pins from said pinlist, create said superset pinout for said family of devices, and mark each pin of said superset pinout associated with each member of said family of devices, wherein said superset listing of pins is generated by reducing layout and footprint changes on a board connected between each member of said family of devices.